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Analysis and Design of Two Stage CMOS Operational Amplifier in 90nm CMOS Technology with High Gain and Low Power Dissipation

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Abstract—*The main concern in modern Integrated Circuit technology is given towards the power dissipation and gain of any electronic device for the applications where very small magnitude signals are to be processed. With the advancement of the CMOS technology, supply voltages are decreasing while at the same time the transistor threshold voltages are almost remaining constant. Operational Amplifier (Op-Amp) is widely known device for providing the high gain. In this paper two stage op-amp has been designed in 90nm technology. To maximize the gain, sizing of various transistors has been optimized. The designed two stage Op-Amp has gain of 46.037 db, phase margin of 66° and CMRR of 60db for 1pf load. It typically exhibits a 20MHz unity gain frequency for 25µA external bias current.*

1. INTRODUCTION

Today 's era the trend of low power low voltage silicon chip systems has been growing due to the increasing demand of portable and battery operated devices with smaller area and longer battery life time[1].In analog electronics world the op-amp plays a significant role.It has a linear characteristics, which is essential in almost all devices. Some of the applications of op-amps are in preamplifiers, buffers, voltage comparators and differential amplifiers, integration and differentiation [2]. At submicron levels the designing of such circuits becomes extremely difficult due to sensitivity of the circuit and trade off with various parameter[3].for faster speed, the supply voltage(vdd) is scaled down to enhance device reliability and to reduce power consumption, as the feature size of CMOS devices keeps shrinking. Higher transition frequency is obtained by downward scaling in gate length, and hence faster transistor's inherent open loop gain(gmro)[2][1].the threshold voltage of transistors does not scale well along with device scaling, which results the shrinking voltage headroom for the amplifier[2][1].In this paper two stage CMOS comparator has been simulated in 90nm CMOS technology for increasing the gain by changing the width of the transistors of circuit. In designing of op-amp, there is trade off between gain and bandwidth. The high gain is achieved by cascading, causes the reduction in the output signal swing[4] Along with gain the CMRR phase margin slew rate have been found out. Two stage op-amp is used to increase the gain of the circuit while another hand frequency compensation is needed for this circuit to make the system stable. There are many techniques for frequency compensation, however single miller frequency compensation technique has been used in this circuit. Compensation techniques are generally robust and offer advantages such as: (i) pole splitting (ii) Left-half-plane(LHP) zero creation and its accurate placement through a null resistor. (iii)In the case of cascade compensation, eliminating the feed forward path due to the presence of a current buffer. Fig(1) shows the block diagram of op-amp.

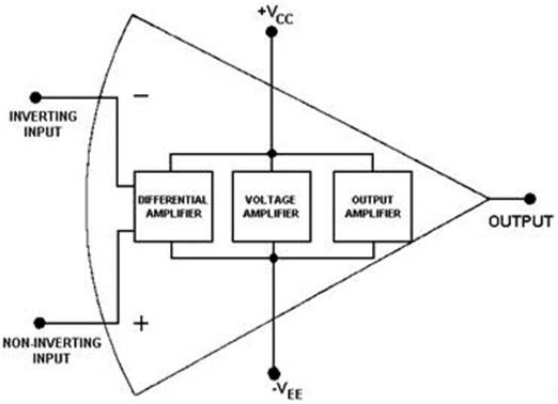

Fig. 1: Block diagram of op-amp

This paper is organized as follows: In section II the description of two stage op-amp is discussed. Section III the designing procedure has been discussed with some equations.

In section IV simulated results are shown by some tables and our contribution is described.

2. CIRCUIT DESCRIPTION

The two stage op-amp is most widely used architecture in ADC shown in figure(3). In which first stage consists of differential amplifier that will convert differential input voltage to differential current. At current mirror load this differential current are applied. Second stage consists of common source MOSFET, converting the second stage input voltage to current. The another transistor M7(current sink load) is used to convert a current to voltage at output node. Second stage is used to provide large swings. It performance and experimental results compare closely to the design specification .In single stage op-amp there is no need of frequency compensation with stable system but some applications required a high gain for that the stage of op-amp is increased. Increasing the stages makes the system unstable. To make the system stable along with high gain, single miller compensation technique has been used shown in figure (2).

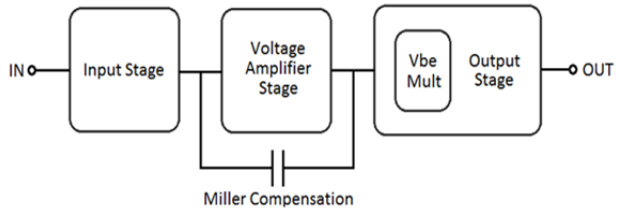

Fig. 2: Single miller compensation technique

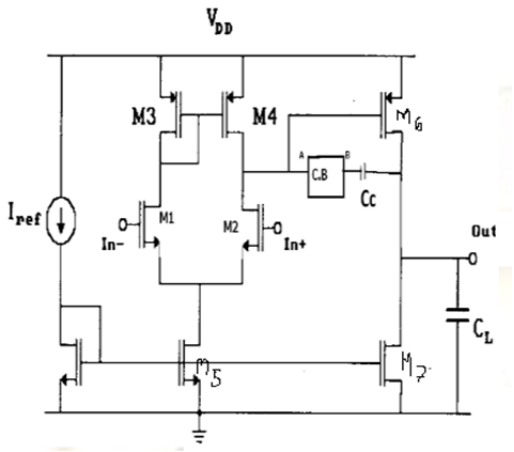

Fig. 3: Circuit diagram two stage open loop comparator.

3. CIRCUIT DESIGN PROCEDURE

The proposed circuit of two stage amplifier is Shown in figure(3).The design procedure of first stage as well as second stage of op-amp are,

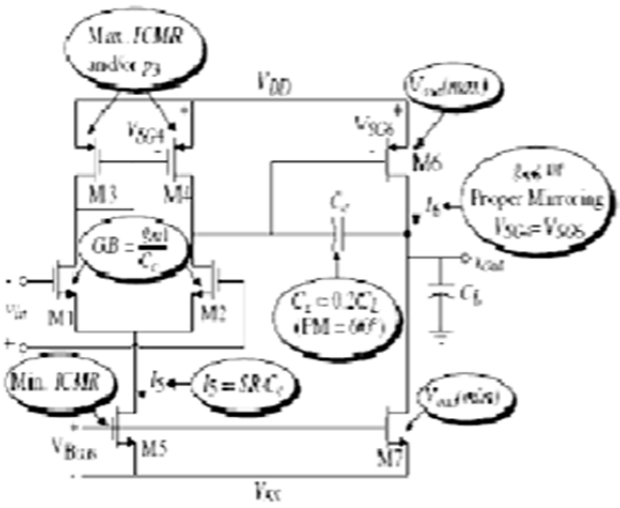

Fig. 4: Illustration of the design relationship and the circuit for a two stage op-amp

Specifications-

Open loop gain (Av)

Minimum input common mode range(Vicm-)

Maximum input common mode range(Vicm+)

Load capacitance (c_L)

Output voltage swing

Swing rate

Design steps-

Step(1) choose the value of c_L and will check later. This value must lie between 1pF and 2pF.This value of output capacitance of the first stage and the slew rate we can find the tail current or bias current (I_5).

Cc>=0.22Cl (1)

Step(2) Determine the value of the current I5 in transistor M5.

$$SR = I_5 / C_c$$

$$I_5 = C_c \times SR \quad (2)$$

Step(3) Design the transistor M1 and M2 by using the current calculated above,

$$(W/L)_{1,2} = \frac{g_{m1}^{2}}{\mu_n c_{ox} 2 I_{D1}} \quad (3)$$

Step(4) design the transistor M3 and M4 by choosing the value of (ICMR+) and finding out the value of Vt3max by using the cadence tool-

$$(W/L)_{3,4} = \frac{2I_{D3}}{\mu_p c_{ox}[V_{DD} - (ICMR+) - V_{t3\max} + V_{t1\min}]^2} \quad (4)$$

Step(5) Design the transistor M5 first calculate Vds5 using the specification of minimum input common mode voltage. The relation is given by

$$V_{Dsat} \geq ICMR\ (-) - \frac{2I_{D1}}{\beta_1} - V_{t1\max} \quad (5)$$

Using the above calculated value of vds5 we can design the transistor M5,

$$(W/L) = \frac{2I_{D5}}{\mu_n c_{ox}(V_{Dsat})''2} \quad (6)$$

Step(6) design transistor M6 by calculating the gm6 and gm4,for calculating gm6 consider the phase margin more than 45^o ,region being in two stage op-amp if the phase margin is lesser then 45 it will give ringing effect which makes the system unstable,

$$g_{m6} \geq 10 g_{m1} \quad (7)$$

$$g_{m4} = \sqrt{\mu_p c_{ox}(W/L).2I_D} \quad (8)$$

$$(W/L)_6 = \frac{g_{m6}}{g_{m4}}(W/L)_4 \quad (9)$$

Step(7) Design transistor M_7 , first calculate the current I_6 ,

$$I_6 = I_7$$

$$\frac{I_6}{I_4} = \frac{(W/L)_6}{(W/L)_4} \quad (10)$$

$$\frac{I_7}{I_5} = \frac{(W/L)_7}{(W/L)_5} \quad (11)$$

4. SIMULATION RESULTS

TABLE I

Design Specifications

S. No.	Parameters	Value
1.	Open loop gain	46.037db
2.	Gain bandwidth product	20Mhz
3.	ICMR(+)	0.8v
4.	ICMR(-)	0.5v
5.	Phase margin	60
6.	Slew rate	20v/u.sec
7.	Load capacitance	2pF
8.	Vdd	1v

TABLE II

Values of w in reference circuit-

Name	W
W 1,2	15u
W 3,4	25u
W 5	20u
W 6	25u
W 7	13.756u

TABLE III

Effect of width of transistors on gain

I_{dc} (μA)	$W_{1,2}$ (μm)	$W_{3,4}$ (μm)	W_5 (μm)	W_6 (μm)	W_7 (μm)	Gain (db)	Power dissipation(μW)
30	15	20	10	20	15	23.63	62.18
30	15	20	10	25	13.75	31.4	67.67
30	15	30	25	25	13.75	45.93	56.52
30	15	25	25	25	25	46.03	58.47

Obtained value of gain-

Practical value of gain is 46db

Theoretical value of gain is 45.67db

Simulated circuit diagram of two stage of open loop comparator

Simulation result-

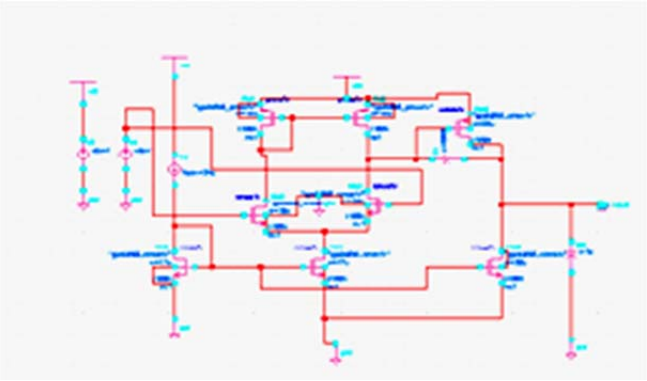

Fig. 5: two stage open loop comparator

Gain obtained-

Gain obtained by simulation is 46.0317db. The upper graph (Fig6) shows the gain and lower graph shows the phase margin (Fig7).

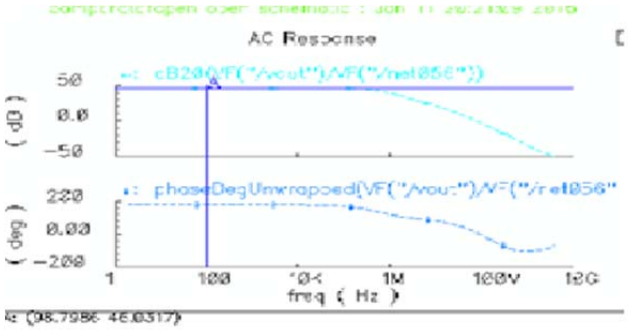

Fig. 6: Open loop gain of Op-amp

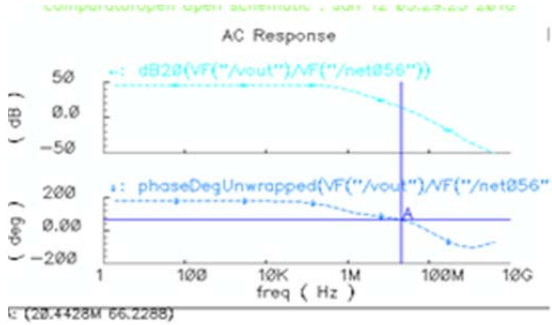

Fig. 7: Phase margin of op-amp

Power dissipation-Power dissipation of whole circuit obtained is 59.9895u in 90nm CMOS technology.

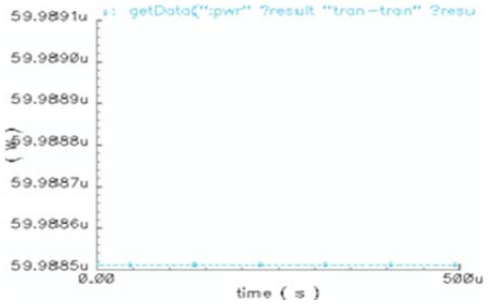

Fig. 8: Power dissipation of whole circuit

CMRR(common mode rejection ratio)-

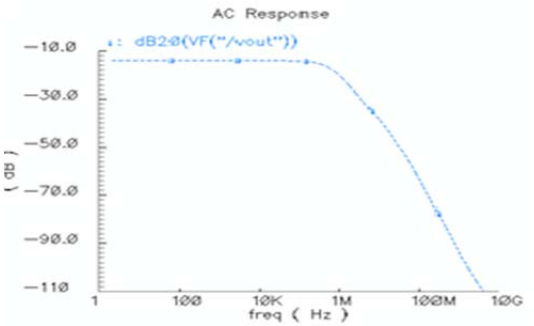

Fig. 8: Common mode rejection ratio

TABLE IV

Comparison of obtained simulation results after sizing in 90nm technology with 130nm and 180nm technology. Phase margin should be high to avoid ringing effect, obtained gain is enhanced as compare to previous work along with improved power dissipation.

Parameter	This Work	90 nm	130nm	180nm
Open loop gain (db)	46.032	31	32	35.73
Unity gain BW (MHz)	20	7.63	5.95	6.997
Phase margin (deg)	66.22	75.287	75.007	75.50

5. CONCLUSION

In this paper a designing of two stage open loop comparator has been done to increase the gain of op-amp by varying the different transistor width. The gain obtained practically is 46.037db while actually it is 45.06db in 90nm technology at 20MhzGBW and power dissipation is 59.885u.The disadvantage of using two stage op-amp, it reduces the stability of device so to improve the stability a single miller compensation technique is used. The gain further can be improved by using the three stage or multiple stage in Op-Amp.

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